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ATTORNEY DOCKET NO.: 00-BN-051 (STMI01-00051) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	ANTHONY X. JARVIS, ET AL.
U. S. Serial No.	:	09/751,372
Filed	:	December 29, 2000
Title	:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Art Group Unit	:	2183
Examiner	:	Aimee J. Li

MAIL STOP APPEAL BRIEF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Reply Brief; and
2. Postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP APPEAL BRIEF-PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 19, 2007.

Date: 11-19-2007 _____
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Date: 11-19-2007 _____
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REPLY BRIEF

Sir:

In response to the Examiner's Answer mailed September 18, 2007, the Applicants submit the following Reply Brief.

ARGUMENT

The Examiner's Answer states:

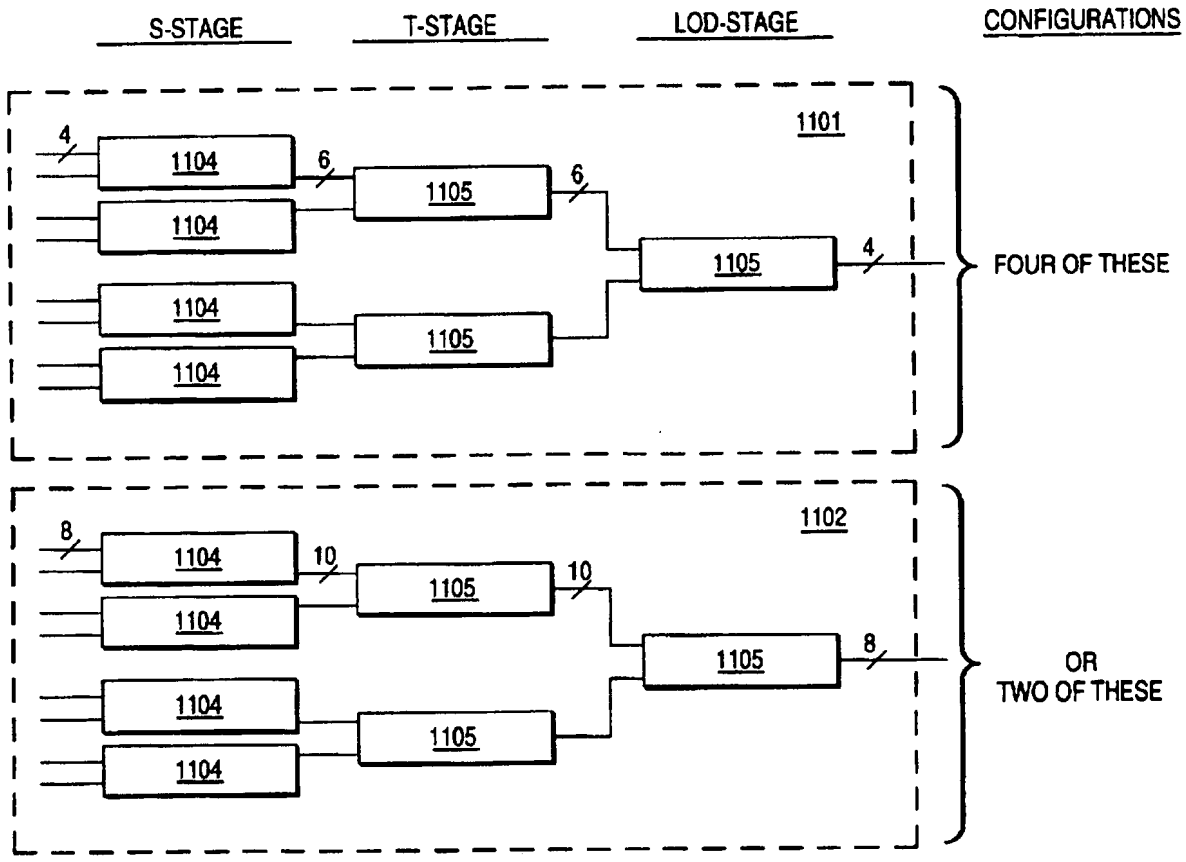
> Hannah clearly discloses that their sign extension unit performs alignment, similar to Greenley, but the system can bypass the sign extension depending on the location of the most and least significant bits in the data word, i.e., whether the most and least significant bits are correctly aligned in the data word. When the most and least significant bits are in the correct positions, i.e., when the significant bits are aligned properly, the sign extension is bypassed, otherwise the sign extension is performed (Hannah column 9, lines 31-67 ". . . Since each slice handles both sign bit and its extension, as well as fraction bits, these capabilities are disables [sic] or bypassed as appropriate for the position of the slice in the larger word . . .").

Examiner's Answer, pages 20-21. However, the very language quoted by the Examiner from Hannah establishes that the Examiner's interpretation of Hannah is incorrect. The phrase "as appropriate for the position of the slice in the larger word" refers to the fact that Hannah teaches using "modular" linear interpolators each acting on a separate "slice" during performance of a 16-bit tri-linear interpolation between two operands:

> It has been determined that to maintain error at less than ±1.0 LSB at the LOD interpolator output, the two fraction bits kept and rounding is performed using the third, at the output of the multiply is necessary. Maintaining two fraction bits builds error to ±3/4 in the currently preferred embodiment, each linear interpolator is "sliced" to allow for 4, 8 or 12-bit data. The first stage of interpolators only need to handle 4-bit input data, The second and third stages are comprised of a slice that handles 6-bit input data.

Hannah, column 9, lines 21-29. Among the implementations suggested by Hannah are a first embodiment employing four identical modular interpolator units each receiving blocks of four bits from each 16-bit operand and a second embodiment employing two identical modular interpolator units each receiving blocks of eights bits from each 16-bit operand:

FIG. 11



Hannah, Figure 11, column 9, lines 30-35. Since the operand's sign is represented in the most significant bits of each operand while any fraction is represented in the least significant bits, only the modular interpolator units handling the most significant bits need perform sign computations and only the modular interpolator units handling the least significant bits need perform fractional computations:

> Since each slice handles both a sign bit and its extension, as well as fraction bits, these capabilities are disabled or bypassed as appropriate for the position of the slice in the larger word. For example, for 8-bit texels, the MS slice would handle the sign bit (and no fraction bits) and the least significant (IS) slice would handle the fraction bits (but no sign). The slice configuration muxes separately enable or disable the slices MS portion (sign extension) or LS portion (fraction).

Hannah, column 9, lines 56-64. Thus, sign computation function or fractional computation function of a given modulator interpolator unit is "disabled or bypassed" when that modular interpolator unit is not operating on a "slice" including the sign or fraction bits – but basic interpolation between the two operands IS still performed on the received slices. Thus, the Examiner's Answer is incorrect in asserting that the cited portion of Hannah establishes that Hannah "performs alignment, similar to Greenley" – to the contrary, the cited portion of Hannah establishes that alignment is not necessary, since each modular interpolator unit is configured to perform sign computations or fractional computations, and thus can accommodate any operand "alignment." Moreover, the cited portion of Hannah also establishes that Hannah does NOT, as suggested in the Examiner's Answer, teach bypassing the interpolation units 1101 or 1102. Instead, Hannah merely teaches disabling or bypassing a portion of the computation performed in each modular interpolator unit, not the entire computation or the entire interpolation unit.

The Examiner's Answer further states:

> Applicants' arguments insinuate that Greenley suggests that data must be processed by the sign extension unit and aligning unit all the time, even when the data is aligned. However, Greenley clearly states that processing through the sign extension unit is only necessary when the data is not properly aligned.

Examiner's Answer, page 21. No support in Greenley is found for the assertion that "Greenley clearly states that processing through the sign extension unit is only necessary when the data is not properly aligned." The Examiner's Answer identifies no support within Greenley for the asserted teaching, and no such support has been found by the Applicants after careful review. Greenley seeks to improve latency by implementing a single pipeline for three different types of LOAD operations: signed LOADs requiring two cycles, unsigned LOADs requiring only one cycle, and data-dependent

signed LOADs requiring either one or two cycles, depending on whether the sign is positive or negative:

> In order to handle the scheduling of the processor 100 pipelines to execute signed and unsigned LOAD instruction in a variable number of cycles, the following rules are implemented by one embodiment of the present invention: in the opcode implementation, signed LOAD instructions are scheduled to execute in two cycles; unsigned LOAD instructions are scheduled to execute in one cycle; signed LOADs in the data dependent scheme, on the other hand, are scheduled to execute in one or two cycles depending on whether the load data is positive or negative. If the signed load data is positive, the processor's pipelines are scheduled to execute the positive signed LOAD instruction in one cycle. Negative signed LOAD instructions are executed in two cycles. In order to execute positive signed LOAD instructions in one cycle, the value of the load data is assumed to be positive and is sign extended by zero-filling the register in much the same manner as unsigned loads are handled by the sign extension unit.

Greenley, column 5, lines 25-42. However, a single pipeline including an aligning unit 170 and a sign extension unit 160 is employed to perform all three types of LOADs:

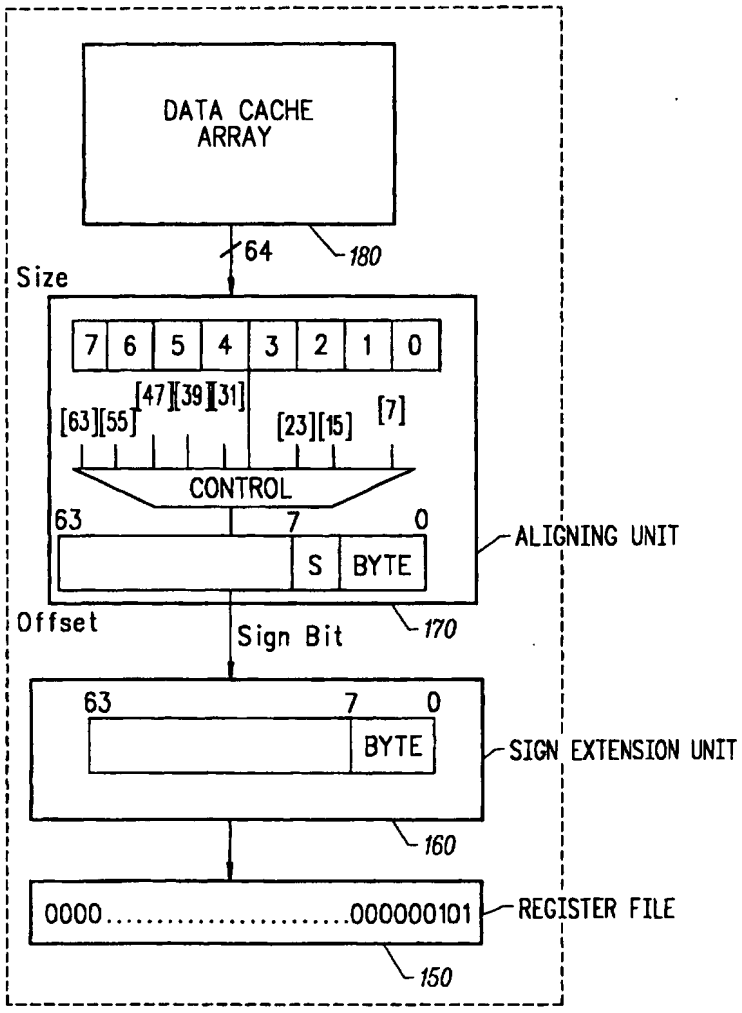


FIG. 2

Greenley, Figure 2, column 5, lines 3-5. As apparent, there is no bypass path around aligning unit 170 and sign extension unit 160 depicted or described in Greenley. Thus, Greenley contains no support for the assertion in the Examiner's Answer that "processing through the sign extension unit is only necessary when the data is not properly aligned." Every operation within the pipeline depicted involves processing by the aligning unit 170 and the sign extension unit 160.

The Examiner's Answer also states:

> Similarly, Hannah has a sign extension and alignment unit for aligning data when the data is out of alignment, as required by Greenley, but further discloses that the sign extension and alignment unit is bypassed only when the data is already aligned, which makes the system faster since unneeded elements and functions are skipped.

Examiner's Answer, page 21. However, Hannah makes no mention of conditional alignment of operands and, as already detailed above, teaches using the sign computation or fractional computation functions of identical modular interpolator units each operating on a "slice" of a larger operand only when the slice contains the sign (the most significant bits) or the fractional portion (the least significant bits). The assertion within the Examiner's Answer is not supported by either of the cited references.

The Examiner's Answer continues to assert that latency savings with result from the proposed combination of Greenley and Hannah, stating:

> As explained in the rejection above, the LOAD instruction takes two cycles, as stated by Greenley in column 4, lines 17-20. *Greenley has taught this two-cycle latency for all load instructions, including those without the need for sign extension.*

Examiner's Answer, pages 21-22 (emphasis added). This assertion is flatly contrary to the actual teachings of Greenley. Greenley teaches, for example, that positve signed LOAD operations are performed in one cycle while negative signed LOAD operations are performed in two cycles:

> In one embodiment of the present invention, the pipeline shown in FIG. 4A executes positive signed LOAD instructions in one cycle and negative signed LOAD instructions in two cycles.

Greenley, column 5, lines 58-61. The portion of Greenley cited in the Examiner's Answer (column 4, lines 17-20) is part of the "Background of the Invention" and relates to problems purportedly overcome by the system disclosed in Greenley.

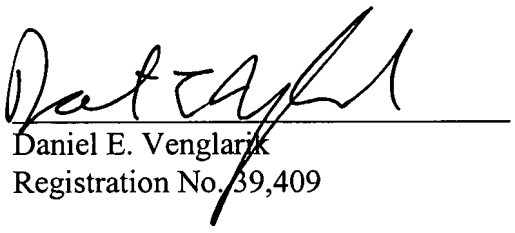
In addition, the mechanism employed by Greenley to accommodate difference latencies (stalling the pipeline, see column 6, lines 6-8) differs from bypassing the shifter circuit to load a data value from the cache directly to the target register without processing the data value in the shifter circuit as recited in the present claims.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,
MUNCK BUTRUS CARTER, P.C.

Date: 11-19-2007



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